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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/605,082 | 09/08/2003 | MIN-LUNG HUANG | 10228-US-PA | 2081 |

31561 7590 04/26/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

| EXAMINER | |
|---|---|
| TSAI, H JEY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,082 | HUANG ET AL. | |
| | Examiner | Art Unit | |
| | H.Jey Tsai | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 9-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Election/Restriction***

Applicant's election without traverse of claims 9-16 in Paper filed on Feb. 17, 2004 is acknowledged.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kwon 2004/0012081 (Applicants may submit an English translation for consideration of the foreign priority over this reference).

Kwon discloses a chip structure, which includes:

a substrate 502/503 having an upper surface, fig. 7,

a die 501 (called active device) having an active surface and a back surface, wherein the active surface is implemented with a plurality of bonding pads, figs. 6a, 7-8, and para. 44-52,

an under-bump-metallurgy layer of composite metals (not shown in the figure) disposed over the bonding pads 501a, see para. 51 and fig. 8,

a plurality of solder blocks 610 respectively disposed above the under-bump-metallurgy layer, fig. 8 and para. 51,

a passive component 102b/102c/104b/104c having a plurality of terminal electrodes, which is coupled to the UBM layer through the solder blocks 610, fig. 8,

a patterned dielectric layer 501b has a plurality of openings that expose the bonding pads 501a and the UBM layer is disposed above the patterned dielectric layer 501b, see para. 51 and fig. 8,

a re-distribution layer 501c is connected to the bonding pads 501a, para. 50 and fig. 8,

a packaging plastic (called resin) 540 enclosing the die 501, the passive component 102b/102c or 104b/104c, and the conductive wire 504c, 504d, para. 046.

Claims 9-11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lin 2004/00029404 (Applicants may submit an English translation for consideration of the foreign priority over this reference).

Lin '404 discloses a chip structure, which includes:

a die 10 having an active surface and a back surface, wherein the active surface is implemented with a plurality of bonding pads 16, figs. 10-11, 2-5 and para. 137-140,

an under-bump-metallurgy layer 50 of metal disposed over the bonding pads 16, see para. 137,

a plurality of solder blocks 52 or 56 respectively disposed above the under-bump-metallurgy layer 50,

a passive component 54/53 of capacitor or inductor having a plurality of terminal electrodes, which are respectively coupled to the UBM layer 50 through the solder blocks 52 or 56,

a patterned dielectric layer 18 has a plurality of openings that expose the bonding pads 16 and the UBM layer 50 is disposed above the patterned dielectric layer 18, fig. 10 or fig. 11,

a re-distribution layer 13 is connected to the bonding pads 16, para. 59.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10, 12-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunimatsu et al. 5,767,564 in view of Ratificar et al. 2003/0121958 and Nguyen et al. 6,238,949.

The reference(s) teach the features :

Kunimatsu et al. substantially discloses a chip structure and a chip package structure, which includes :

a substrate 1 (called package) having an upper surface, fig. 1+ and col. 3, lines 34+,

a die 2 (called semiconductor element) having an active surface and a back surface, wherein the back surface of the die 2 is in contact with the upper surface of the substrate 1 (called package) and the active surface is implemented with a plurality of bonding pads, see fig. 2-3, and col. 4, lines 13+,

a solder block 3A disposed on the die 2, figs. 2-3 and col. 4, lines 32+,

a passive component 3 (a capacitor) with a plurality of terminal electrodes 5, 7, 8 wherein the terminal electrodes are coupled to the solder block 3A, col. 4, lines 38+,

a plurality of conductive wires electrically connecting the die 2 and the substrate 1.

Ratificar et al. teaches at figs. 1a-1e and para 16-26 and 38, a pattern dielectric layer 120 to form a via opening exposing the bonding pad 110, UBM layer 130 including gold formed over dielectric layer 120 and solder block 150.

Nguyen et al. teaches at col. 1, lines 15-22, col. 3, lines 34-38 using a plastic as an encapsulant for a chip package.

The difference between the reference(s) and the claims are as follows: Kunimatsu et al. teaches mounting a passive component of capacitor to a chip through a solder block but does not teach that a UBM and a bond pad are commonly formed under solder block and using plastic to encapsulate the die. However, Ratificar et al. teaches at para. 16-26 and 38 and fig. 1d-1d, a UBM layer 130 and a bonding pad 110 formed under the solder block 150. And, Nguyen et al. teaches at col. 1, lines 15-22, col. 3, lines 34-38 using a plastic as encapsulant to form a packaged integrated circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Kunimatsu et al.'s process with a UBM, a bonding pad as suggested by Ratificar et al. and using a plastic package as suggested by Nguyen et al. because UBM can promote the adhesion of the solder block to the bonding pad and bonding pad provides a larger surface for making connection between the interconnection layer in the die to solder block, and plastic package is less expensive than other type of chip package.

Claims 11 and 14 are rejected under 35 U.S.C 103 as being unpatentable over Kunimatsu et al. in view of Ratificar et al. and Nguyen et al. as applied to claims 9-10, 12-13 and 15-16 above, and further in view of Lin 6,303,423.

The difference between the references applied above and the instant claim(s) is: Primary reference Kunimatsu et al. in view of Ratificar et al. and Nguyen et al. does not teach a re-distribution layer is connected to the bond pad. However, Lin '423 teach at col. 7, lines 37-53 and figure 4 and 11 that a network of electrical connections formed from conductive line 13 is connected to bonding pad 16.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with a re-distribution layer as taught by Lin '423 because passive component formed over the die can be re-distribute to the circuit formed in the die.

**Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is 571-272-1626 and Fax number (703) 872-9306.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

hjt

4/20/04

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800